

This listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

- 1           1.       (original) A programmable logic device (PLD) comprising:  
2   input/output (I/O) interface having a first plurality of I/O register blocks, the first plurality of I/O  
3   register blocks being partitioned into a second plurality of I/O sections each I/O section having N  
4   data I/O register blocks and a strobe circuit, wherein each of the N data I/O register blocks is  
5   configured to store multiple bits of data, and each strobe circuit is configured to generate a local  
6   strobe signal that drives a local clock line coupling to clock inputs of the N data I/O register  
7   blocks, the N data I/O register blocks and the strobe circuit in each I/O section being coupled to a  
8   corresponding number of device pins; and  
9   programmable logic circuitry coupled to the I/O interface.
- 1           2.       (cancelled) The PLD of claim 1 wherein the strobe circuit in each I/O  
2   section is configured to shift a phase of an input strobe signal received at a respective strobe pin.
- 1           3.       (cancelled) The PLD of claim 2 further comprising a master phase control  
2   circuit coupled to receive a master clock signal and configured to generate a phase control signal  
3   that controls a phase delay in the strobe circuit in one or more of the second plurality of I/O  
4   sections.
- 1           4.       (cancelled) The PLD of claim 3 wherein the second plurality of I/O  
2   sections are grouped into a third plurality of I/O banks.
- 1           5.       (cancelled) The PLD of claim 4 wherein a separate master phase control  
2   circuit is provided for I/O sections in each of the third plurality of I/O banks.
- 1           6.       (cancelled) The PLD of claim 1 wherein each I/O register block comprises  
2   two registers, one of which stores a first incoming bit of data at a rising edge of the local strobe

3 signal and the other stores a second incoming bit of data at a falling edge of the local strobe  
4 signal.

1 7. (cancelled) The PLD of claim 6 wherein the strobe circuit in each I/O  
2 section comprises a programmable phase delay circuit that is configured to shift a phase of the  
3 local strobe signal such that an edge of the local strobe signal occurs substantially at the center of  
4 a data pulse.

1 8. (cancelled) The PLD of claim 7 wherein the phase delay is about 90  
2 degrees.

1 9. (cancelled) The PLD of claim 1 wherein each I/O section further  
2 comprises one or more general purpose register blocks coupled to respective device pins.

1 10. (cancelled) The PLD of claim 1 wherein, in each I/O section, the strobe  
2 circuit is located as close to a center the N data I/O register blocks as possible wherein an equal  
3 number of data I/O register blocks are located in either sides of the strobe circuit.

1 11. (cancelled) The PLD of claim 1 wherein the programmable logic circuitry  
2 comprises a plurality of programmable logic blocks coupled via a network of a plurality of  
3 programmable vertical and horizontal interconnect lines.

1 12. (cancelled) A computing system comprising a multiple-data-rate memory  
2 circuit coupled to a programmable logic device (PLD) as set forth in claim 1.

1 13. (cancelled) The computing system of claim 12 wherein the multiple-data-  
2 rate memory circuit comprises a double data rate synchronous dynamic random access memory.

1 14. (cancelled) A method of operating a programmable logic device (PLD)  
2 comprising:

3 receiving N groups of data bits each group having M data signals and a  
4 corresponding data strobe signal;  
5 partitioning I/O register blocks inside the PLD into a corresponding N I/O  
6 modules, each module having M I/O register blocks and a strobe circuit coupled to receive a  
7 respective group of M data signals and data strobe signal; and  
8 driving clock inputs of the M I/O register blocks in each of the N I/O modules using an  
9 independent clock network that is local to each of the N I/O modules.

1 15. (cancelled) The method of claim 14 further comprising programmably  
2 shifting a phase of the data strobe signal before driving the clock inputs of the M I/O register  
3 blocks.

16. (cancelled) The method of claim 15 wherein the programmably shifting of  
the phase of the data strobe comprises generating phase control signal in response to a system  
clock.